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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/773,246	02/01/2001	David Robert Cameron Rolston	AP566US	4340

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EXAMINER	
JAGANNATHAN, MELANIE	
ART UNIT	PAPER NUMBER
2666	

DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/773,246	ROLSTON ET AL.	
	Examiner	Art Unit	
	Melanie Jagannathan	2666	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-13 and 15-18* is/are rejected.

7)☒ Claim(s) *6 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/3/2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5, 7-13, 15-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Miller US 5,712,882.

Regarding claims 1, 7 15-18, the claimed method and apparatus for providing synchronized clock signals at N distributed nodes in system, the nodes comprising a master and plurality of slave nodes interconnected by first and second propagation channels is disclosed by system (Figure 1, element 10) for providing synchronized local clock signals to a set of distributed local modules (elem3ent 12) of a logic circuit with a clock source (element 14) and first and second transmission lines (elements 18, 20). The claimed generating a first pulse train and second pulse train each being regular and having period T and propagating first pulse on first channel and second pulse on second channel in reverse order of each other is disclosed by first transmission line (element 18) routes clock signal CLK output of clock source as a reference clock signal CLKA to each deskewing circuit (element 16) in succession in counter-clockwise order and second transmission line (element 20) routes CLKB to each deskewing circuit in succession in reverse (clockwise) order. See column 3, lines 60-67, column 4, and lines 1-30. The claimed maintaining the rate of each of the pulse trains such that there are pN pulses in each propagation at any time, the pulse of first train arriving simultaneously and the same for second

train is disclosed by although the first and second transmission lines transmit clock signals in opposite directions between deskewing circuits, they have the same length and velocity of signal propagation between adjacent circuit modules. See column 4, lines 1-20. The claimed detecting arrival at detection point of pair of pulses and generating a clock signal event is disclosed by at deskewing circuit CLKA passes through first delay circuit (element 26) and CLKB passes through controller and local clock signal CLKL is produced at a time midway between arrivals of CLKA and CLKB. See column 4, lines 31-67, column 5, and lines 1-42.

Regarding claims 2, 8, 12-13, 15-17, the claimed at each slave node, the step of adjusting delays in each propagation channel when the pairs of pulses do not arrive with the required phase difference such that when each of the slave nodes is generating clock signal events, the propagation time between respective detection points of each pair of adjacent nodes is equal to the propagation time between respective detection points of each other pair of nodes is disclosed by at deskewing circuit, a pulse of CLKA signal arrives after a delay of D1 while CLKB arrives after a delay of D2+D3+D4+D5 and deskewing circuit produces each local clock signal CLKL pulse at the time midway between arrivals of CLKA and CLKB, this is done at all deskewing circuits and so each deskewing circuit produces an output clock signal pulse that is delayed from the CLK output of source by same amount of time so all local clock signals produced by deskewing circuits will have the same phase and frequency. See column 5, lines 13-42.

Regarding claims 3-5, 9-10, the claimed system having delay units in each propagation channel at each slave node, each delay unit comprising pre-delay unit disposed upstream and post-delay unit disposed downstream such that any increment, decrement in pre-delay in one of propagation channels is adjusted by decrement, increment in post-delay in the other of

propagation channels is disclosed by delay circuits in each deskewing circuit (elements 26, 28) and CLKA passes through one delay circuit (element 26) to become local clock for local module and then passes through another delay circuit (element 28) to produce local reference signal REF. CLKB drives controller (element 30) which produces an output signal to control delays in delay circuits such that when REF leads CLKB, controller decreases magnitude of output signal and when REF lags CLKB, controller increases magnitude and this feedback adjusts the delays of delay circuits to phase lock REF to CLKB and local clock signal will have phase midway between phase of CLKA and CLKB. See column 4, lines 31-59.

Allowable Subject Matter

3. Claims 6,14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Prior art of record does not disclose, in single or in combination, the claimed dividing the frequency of first and second pulse trains by an integer multiple of nodes to produce a third pulse train at a lower frequency, propagating the third pulse around nodes via a third propagation channel and adjusting the rate of first and second pulse trains to maintain a predetermined phase relationship between third pulse trains entering the third propagation channel and third pulse train pulses leaving the third propagation channel.

Response to Arguments

4. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. Bedell et al. US 5,734,685 discloses clock signal deskewing system.

Kishi US 5,499,275 discloses clock recovery system capable of automatically switching a direction of clock pulse sequence.

Li et al. US 6,693,985 disclose clock and data recovery system.

Donnelly et al. US 6,539,072 disclose delay locked loop circuitry for clock delay adjustment.

Li US 5,058132 discloses clock distribution system.

Douros et al. US 4,716,575 disclose adaptively synchronized ring network for data communication.

Cerminara US 4,977,581 discloses multiple frequency clock system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Melanie Jagannathan whose telephone number is 571-272-3163. The examiner can normally be reached Monday-Friday 8:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema S. Rao can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-3163.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MJ

FRANK DUONG
PRIMARY EXAMINER